The University of Texas Rio Grande Valley
College of Engineering and Computer Science
Department of Electrical & Computer Engineering

EECE 3230-02 Electrical Engineering Lab II
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Lab Report 1
Analog Pulse and Switching Circuits

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Contents

I. ABSTRACT

In this laboratory exercise, several analog pulse and switching circuits were designed, tested, and analyzed. First, an Input Voltage Source was built using a potentiometer and a voltage follower to generate a controllable voltage in the range of approximately −13 V to +13 V. Next, Comparators Using Standard Op-Amps were constructed and evaluated for their threshold accuracy (e.g., switching at −5 V with outputs of 0 V and +9 V), as well as tested for upper-frequency limitations. A Comparator Using a Comparator Integrated Circuit (LM311) was then analyzed to compare its performance to the standard op-amp comparator. Following that, Circuits with Hysteresis (Schmitt Triggers) were implemented to observe bi-level switching thresholds, and a Design modification introduced asymmetrical thresholds (0 V and +4 V). Further, Pulse Forming Circuits were examined for shaping a sine-wave input into pulses; the Redesign of these circuits tailored the pulse width and amplitude to strict project specifications (−5 V to 0 V at 220 μs width). Finally, a Miller Integrator and Waveform Generator was built and verified, culminating in the Design Problem – Waveform Generator, which combined hysteresis and integration to produce a free-running oscillator meeting specific frequency (220 Hz) and amplitude requirements. All measured results—thresholds, pulse widths, frequency ranges, and output levels—fell within the allowable error margins, demonstrating the versatility and importance of nonlinear analog circuits in practical applications.

II. BODY

INPUT VOLTAGE SOURCE

For lab 1 “In the Lab” section, this group got assigned Project A which will define the later given components or general values of a specified circuit. For the first section of the lab, it was asked to first set up a Dual Power Supply with +15V and -15V by using two channels, the first channel’s positive terminal will be the +15V, then by shorting the first channel’s negative terminal with the second channel’s positive terminal a common ground can be created, finally the -15V can be obtained from the negative terminal of the second channel. After setting up the power supply, the next step is to set up a voltage follower using a TL081 op amp with its Vcc+

going into +15V, Vcc- going into -15V, a feedback loop from the output to the inverting terminal and the non-inverting terminal going into a potentiometer that controls the voltage from +15V to -15V. The voltage follower is important as it lets us sweep a voltage from -15V to +15V which can be used as other op amps inputs that will be used in the later sections of this lab. A schematic of the voltage follower will be included in the following section as the first op amp.

COMPARATORS USING STANDARD OP-AMPS

With the help of the voltage follower, it was asked to design a comparator using standard operational amplifier chips and NOT a special kind of comparator chip. A comparator is a circuit that compares two voltages and outputs a signal indicating which one is larger. Since project A was assigned to our group, the following specifications of our comparator were given: Vout = +9V if Vin > -5V and Vout = 0V if Vin < -5V. The specifications given for the comparator essentially say that the output will become +9V if the input voltage is above -5V and the circuit will output 0V if the input voltage is less than -5V. To design this comparator, another TL081 op amp was used; it is known from the given information that the required input threshold voltage is at -5V when it switches. It is known that a comparator originally switches at the 0V mark for Vin, so it was decided to offset the op amp's reference voltage to -5V so that the switching point is moved to -5V instead of at the origin at 0V. The way this was applied was by using the same -15V from the dual power supply and splitting the voltage so that only -5V is sent to the inverting terminal of the second op amp used as our comparator. To send -5V into the inverting terminal, two resistors were used to split the voltage labeled as R1 and R2, by applying KCL at node V- and knowing that we want 5V to be sent to the negative terminal, we can determine the resistances of R1 and R2 from the R1/R2 ratio we get at the end:

KCL at Node V-

$$I1 = I2$$

$$\frac{-15 - V -}{R1} = \frac{V -}{R2}$$

$$\frac{-15 - 5}{R1} = \frac{-5}{R2}$$

$$\frac{R1}{R2} = -\frac{10}{5}$$

With this derived ratio we can assign R1 = 10k ohms and R2 = 5k Ohms to get -5V at the inverting terminal which changes the switching point at -5V. To get our desired output of 9V when the input is greater than -5V and 0V when the input is less than -5V would be by first adding a diode to only get the +15V when input is greater than -5V and instead of outputting -15V when the input is less than -5V it will instead output 0V because of the diode. Then for the final step, it would be to drop the voltage to +9V from the output +15V at the op amp output by adding resistors R3 and R4 and our output being in between them. The reason for this would be to apply KCL to our output and solve for our missing resistor values with found ratio like before since we know what voltage we want at that node:

KCL at Node Vout

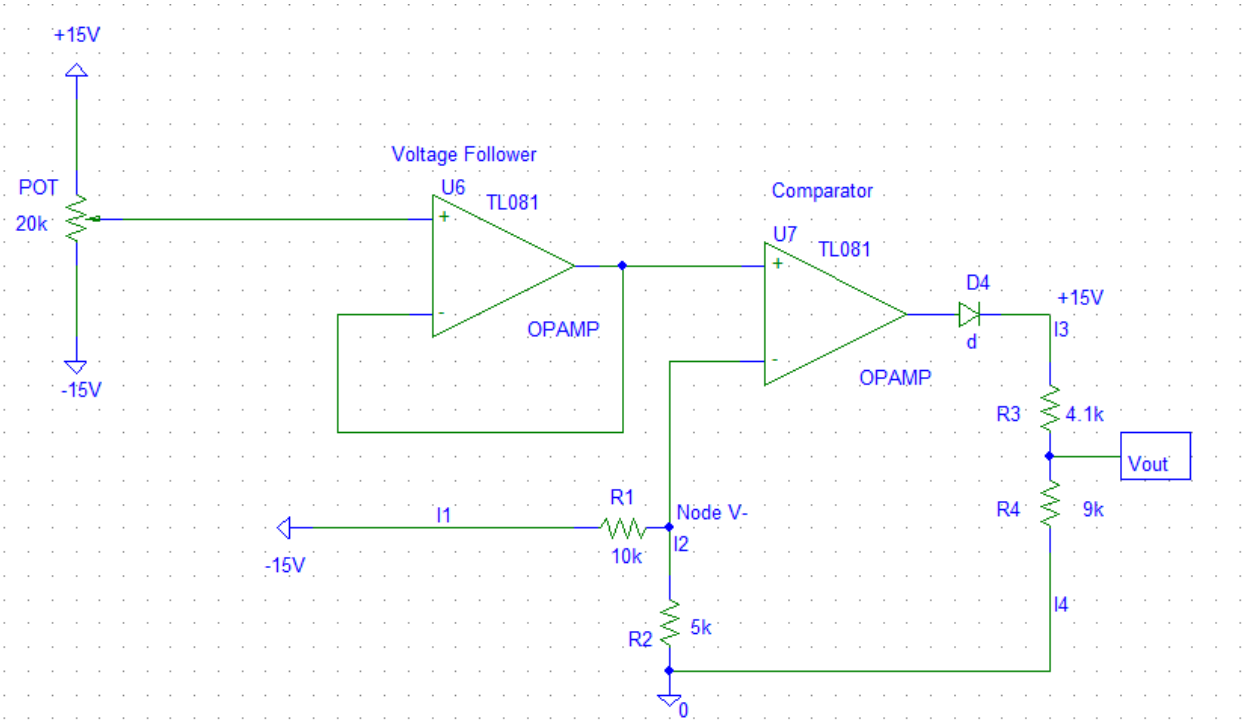
$$I3 = I4$$

$$\frac{15 - Vout}{R3} = \frac{Vout}{R4}$$

$$\frac{15 - 9}{R3} = \frac{9}{R4}$$

$$\frac{R3}{R4} = \frac{4}{9}$$

With this ratio we can assign R3 = 4k Ohms and R4 = 9k Ohms to give us the necessary 9V at the node in between those two resistors which conclude our component calculations for this section (NOTE: We changed the 4k resistor to 4.1k since we wanted the output to be as close to 9V as possible). The following schematic displays the voltage follower and comparator with component values:



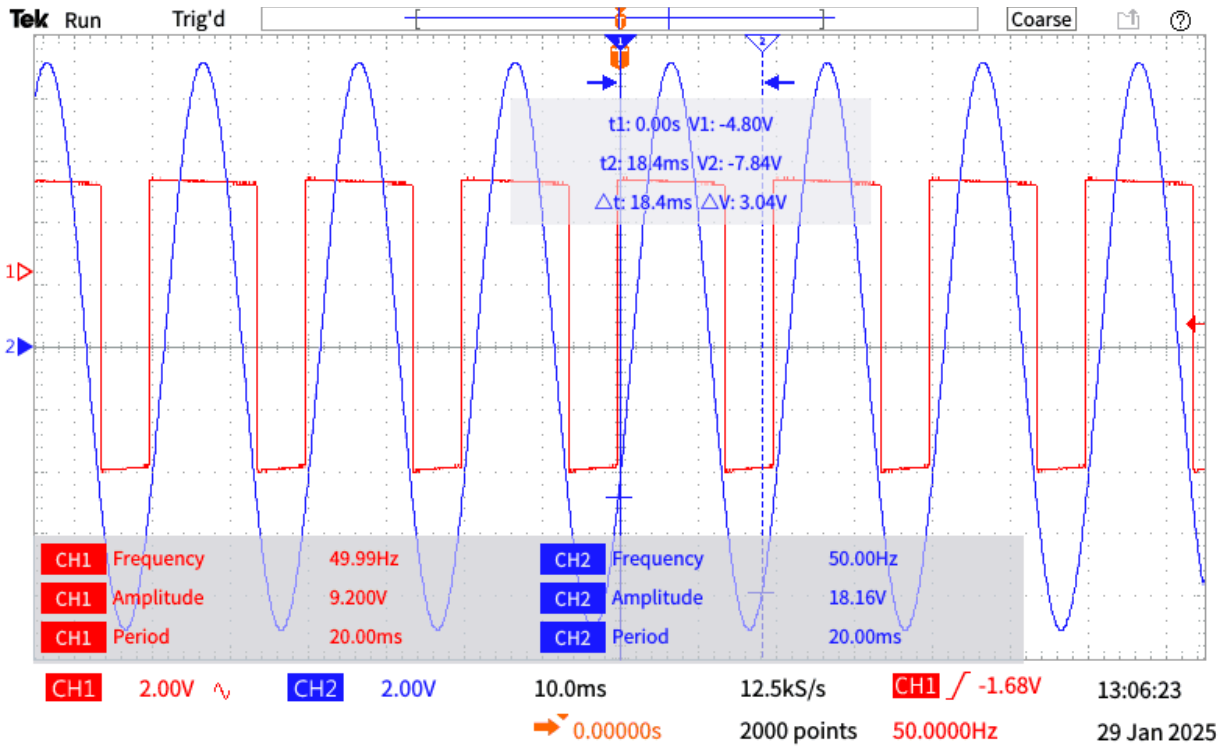
Schematic 1 - Comparator Circuit Schematic Using Standard Op-Amps

For step (3) it was asked to record data showing the Vin threshold voltage in other words the input voltage that makes the output switch according to the specifications given. By testing our circuit, it was observed that the recorded values were correct and within the required input voltage for the output to switch, the following important values were recorded:

Cases	Vin Input	Output Vout
Vin > -5 V	-4.95 V	9.234 V
Vin < -5 V	-5.07 V	0.05 mV

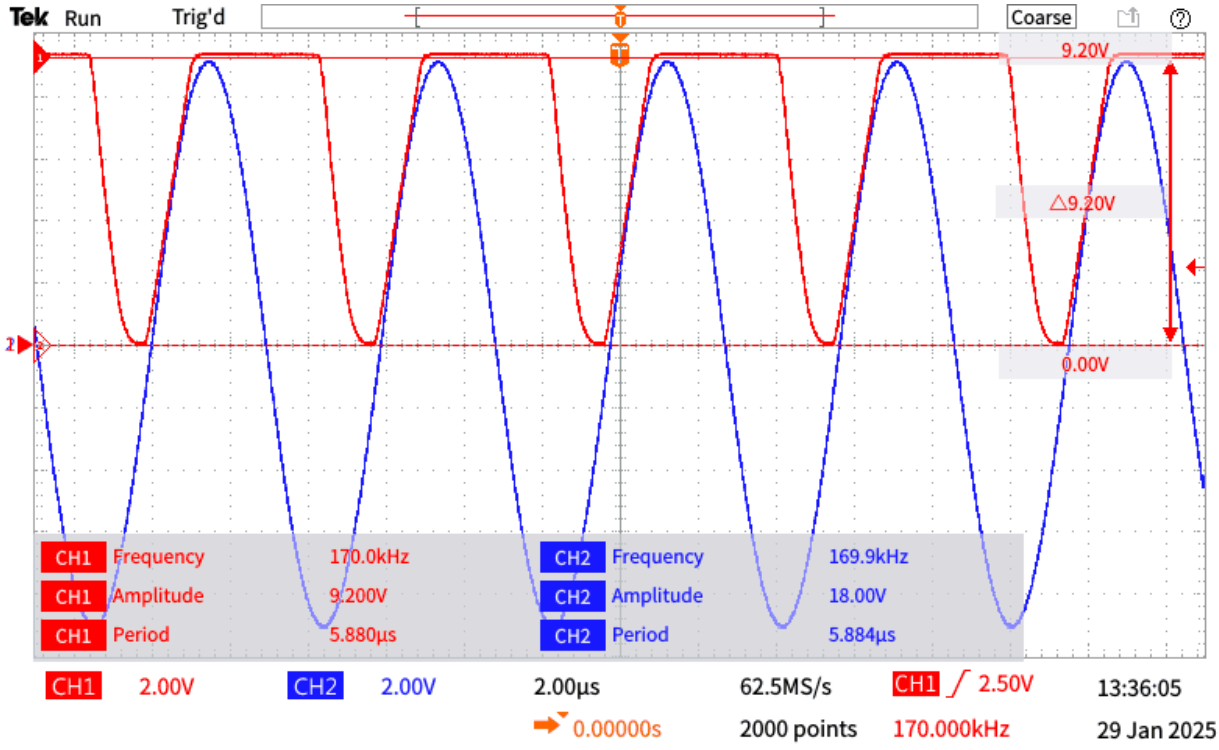
Table 1 - Comparator using standard op-amps recorded output voltage from varying input voltage

For step (4), the following function generator parameters were given to replace the voltage follower which is the input for the comparator op amp with the parameters being 50 Hz, 18 Volts peak-to-peak, and no offset, the following scope shot is of the sine wave input and Vout output:



Scope Shot 1 – Comparator using standard Op-amps Scope Shot of Sine Wave Input (Blue) and Vout output (Red)

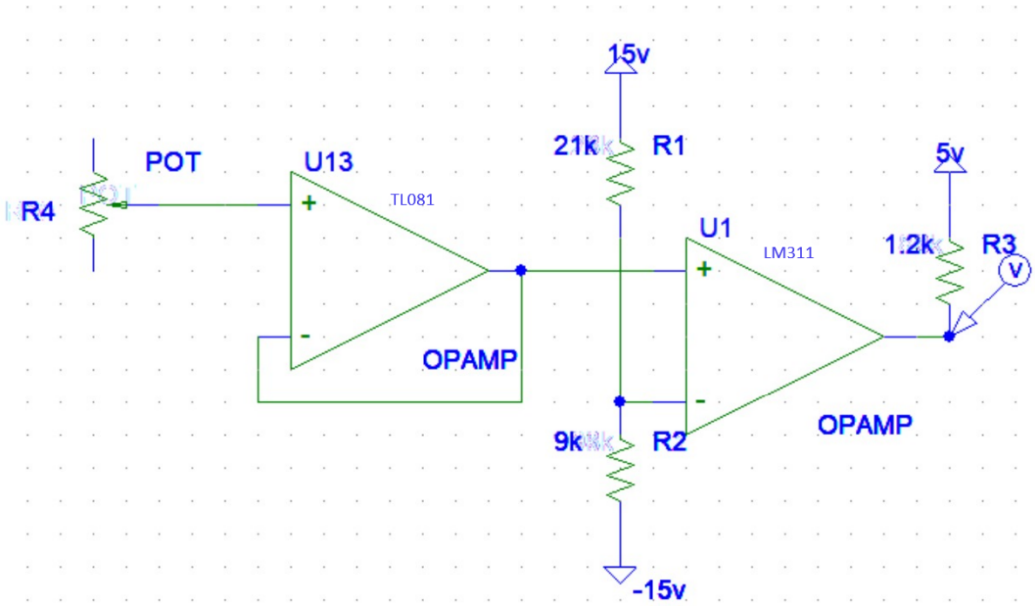
For step (5), the function generator frequency was increased until the circuit stopped working and the way it was known that the circuit stopped working would be when the output cannot stabilize at the specified output voltage level before having to switch which the noted frequency was around 100kHz but more noticeably at 170kHz displayed on the scope shot below:



Scope Shot 2 - Frequency at which the comparator using op amps circuit stops working (170k Hz) shown as Vout output (Red) does not stabilize at 0V

COMPARATOR USING COMPARATOR INTEGRATED CIRCUIT

For this section, it was asked to build a given circuit (Schematic 2) using the LM311 comparator chip and find the values for R1 and R2 to get the input threshold voltage of -6V since project A was assigned to our group to note down the input threshold voltage and outputs before and after the switching points.



Schematic 2 - Given Comparator Circuit Schematic

To find the missing resistances R1 and R2, nodal analysis was performed at the inverting terminal of the LM311 op amp which we'll name V and find the ratio R1/R2 to assign appropriate resistances since the value of V is known to be -6, the required input threshold voltage:

Nodal Analysis at Node V-

$$I1 = I2$$

$$\frac{-V - 15}{R1} = \frac{V - (-15)}{R2}$$

$$\frac{-6 - 15}{R1} = \frac{-6 + 15}{R2}$$

$$\frac{-21}{R1} = \frac{9}{R2}$$

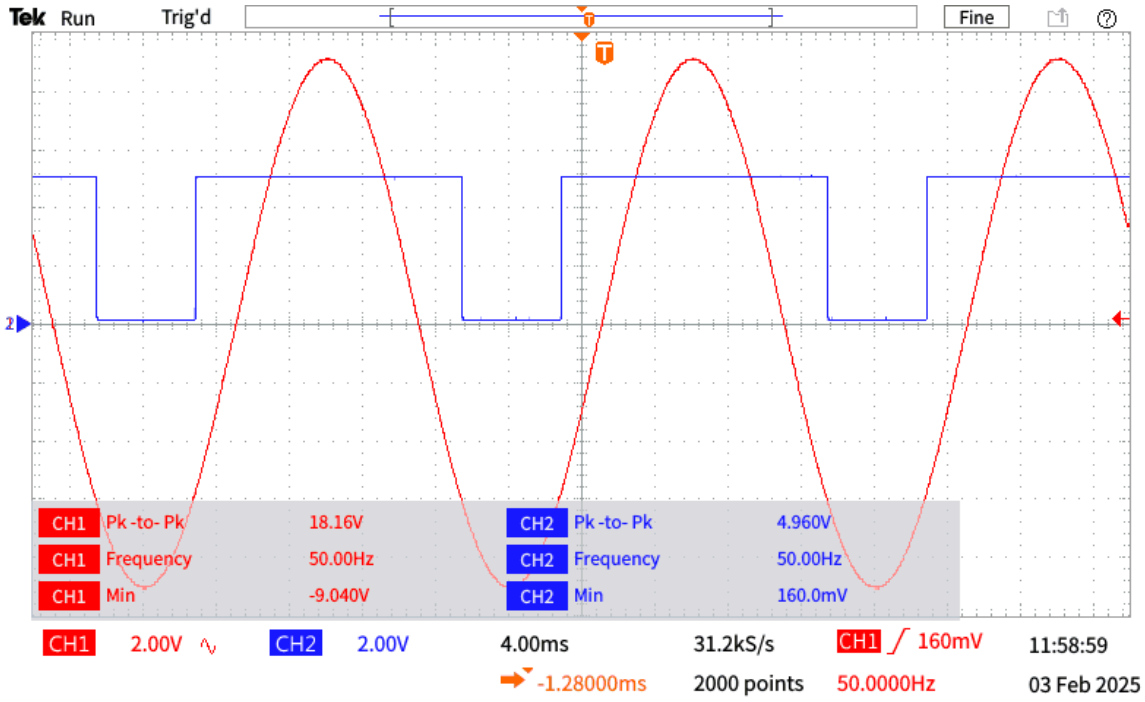
$$\frac{R1}{R2} = -\frac{21}{9}$$

With the found R1/R2 ratio, we can then assign the resistances to be R1 = 21k Ohms and R2 = 9k Ohms to get the required input threshold voltage. For step (7), the observed behavior is the same as the previous comparator section in the sense that the LM311 chip is the comparator itself and the following recorded output change from the input voltage was noted.

Cases	**Vin Input**	**Output Vout**
Vin > -6 V	-5.913 V	4.99 V
Vin < -6 V	-6.093 V	114.42 mV

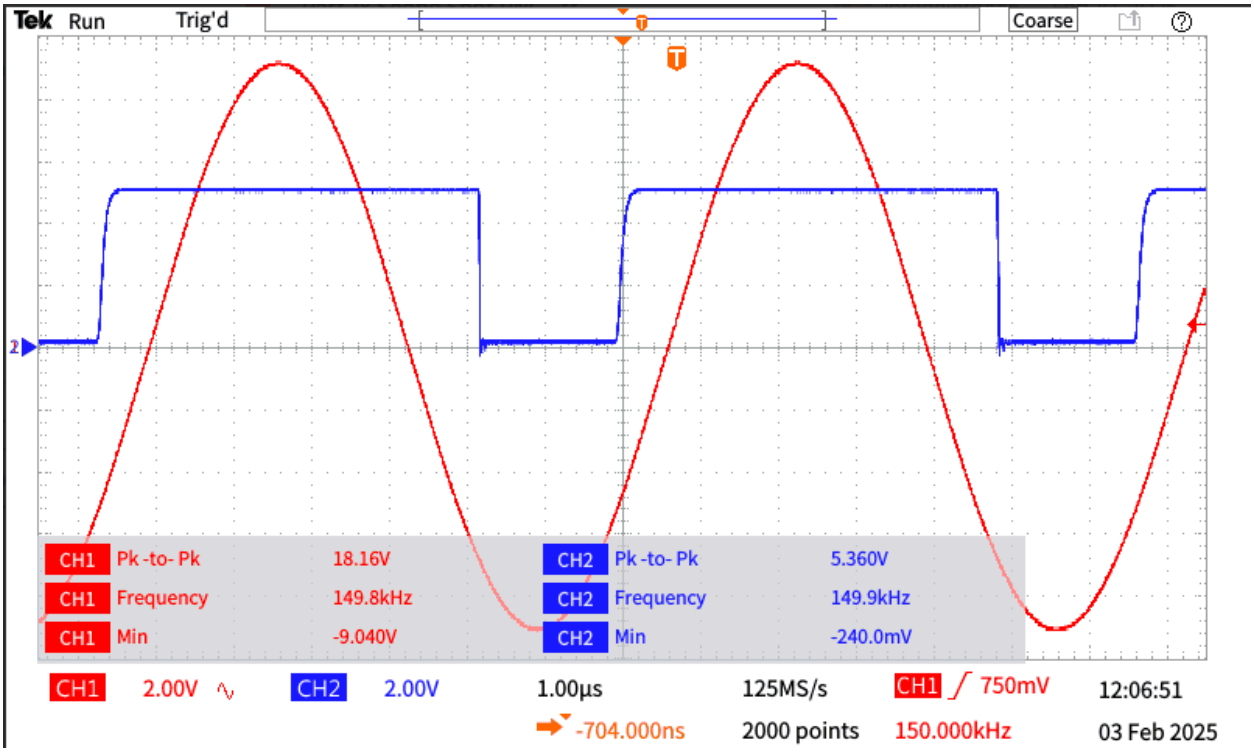
Table 2 - Comparator using comparator integrated circuit recorded output voltage from varying input voltage

For step (8), the voltage follower was replaced by the function generator shown as “IN” in Schematic 2 with the following parameters: 50Hz, 18 V peak-to-peak and no offset, the following scope shot is of that required function generator parameter.



Scope Shot 3 – Comparator using Comparator Circuit Scope Shot of Sine Wave Input (Red) and Vout output (Blue)

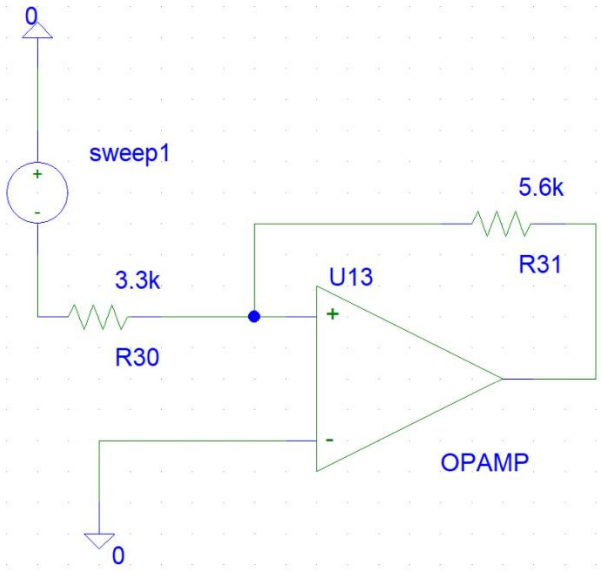
For Step (9), the frequency limit of the circuit was tested just like the previous circuit to observe when the circuit "stops working", in other words, when the output is not stable when switching and the frequency was noted to be 150k Hz. The noticeable difference between this integrated circuit comparator to the op amp comparator output waves would be that for the circuit integrated comparator, the output struggles to stabilize at the peak amplitude of 5V (Scope Shot 3) and for the comparator using op amps, the output struggles to stabilize at the lowest amplitude or when it's at 0V (Scope Shot 2).



Scope Shot 4 - Frequency at which the comparator integrated circuit stops working (150k Hz) shown as Vout output (Blue) did not stabilize at 5V

CIRCUITS WITH HYSTERESIS (SCHMITT TRIGGER)

For this section of the lab, a circuit schematic was given depending on the project letter assigned, since project A was assigned to our team, we got a specific Schmitt trigger circuit schematic displayed below with given resistance values:



Schematic 3 - Schmitt Trigger Hysteresis Circuit

Step (11) asked for us to use nodal analysis and compute the expected value for the two switching threshold voltages. To compute this, it must be noted that for this hysteresis circuit, the moment that V+ = V- that's when the output Vout will change; as a result, since V- = 0V we can say that V+ = V- = 0V for us to use in the following computation. This can be computed using KCL at node V^+ to find out the two switching threshold voltages:

Nodal Analysis at Node V^+

$$I1 = I2$$

$$\frac{Vin - V+}{3300} = \frac{(V+) - Vout}{5600}$$

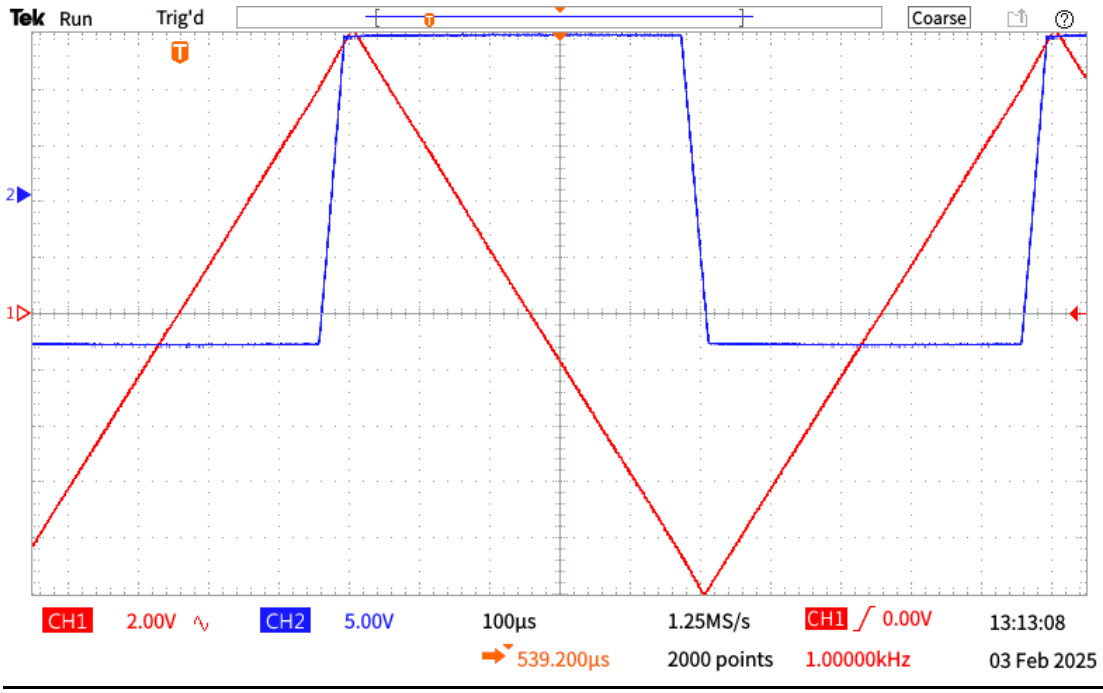
$$\frac{Vin - 0}{3300} = \frac{0 - Vout}{5600}$$

$$Vin = -\frac{Vout * 3300}{5600}$$

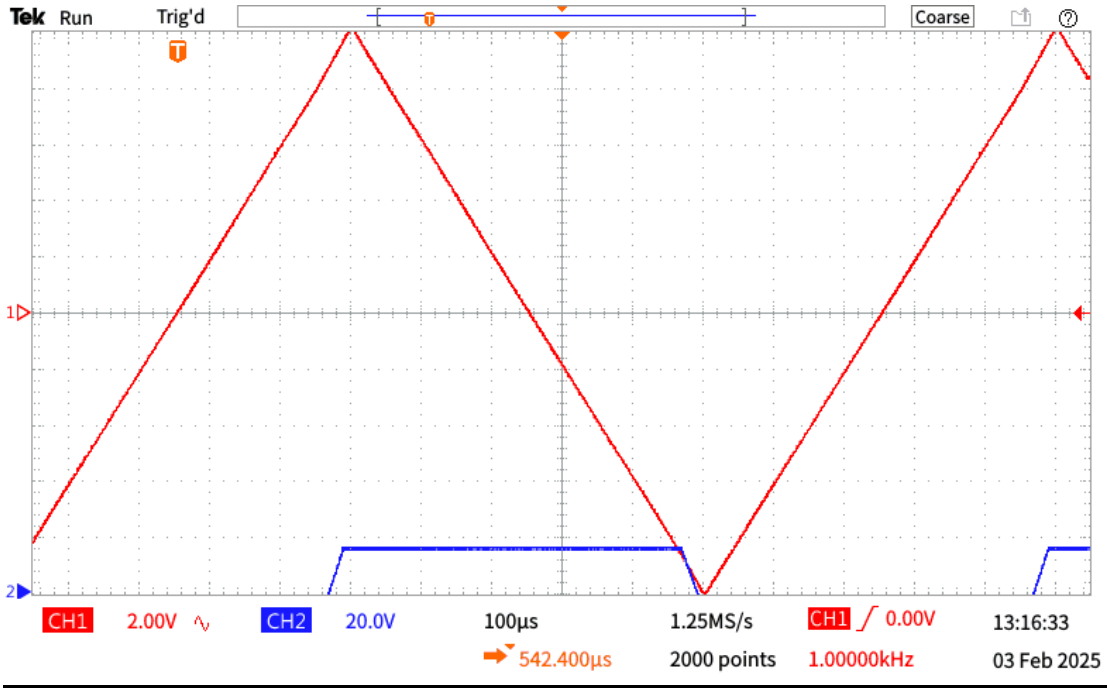
$$Vin1 = -7.66V\ (when\ Vout = 13\ V)$$

$$Vin2 = 7.66V\ (when\ Vout = -13\ V)$$

The two switching threshold voltages found as Vin1 and Vin2 show the two instances where the output changes depending on what direction you sweep the input voltage. For example, if you sweep the input voltage from +13V to -13V you will see that the output changes when the input hits around the -7.66V mark. On the other hand, when you sweep the input voltage from -13V to +13V you will see that the output changes when the input hits the 7.66V mark. For step (12), it was required to do an input voltage sweep to confirm that the switching points are correct, but instead of sweeping it, our instructor Mr. Medina recommended using the oscilloscope as our input and use the ramp wave to check where the switching points happen with a frequency of 1k Hz. The way to check it would be to line up the output left corner side of the high switching point and line it up with the ramp wave to check what voltage is shown there and by using the voltage/division blocks, it can be noted that the positive switching point is around 8 volts (using the 2.00V from the red ramp wave) and for the negative Vin1 when Vout is +13V if we line up the right corner high side of the output with the bottom of the ramp wave it can be observed that the voltage from zero to the corner touching is around -8 volts (using the 2.00V from the red ramp wave). Both will be displayed below:



Scope Shot 5 - Vout output (Blue) Top left corner aligned with input ramp wave (Red) for the estimated ~ +8V



Scope Shot 6 - Vout output (Blue) Top right corner aligned with input ramp wave (Red) for the estimated ~ -8V

CIRCUITS WITH HYSTERESIS – DESIGN

For this section of the lab, it was required to design a Hysteresis circuit like the one that was previously given but with certain input switching points which are +4 Volts and 0 Volts. To design this circuit, it is needed to work backwards compared to the previous section, in other words we have been given the required switching points, but we need to find the resistances that will give us those switching points as well as add additional components to achieve those switching points. To compute and find the resistance values for R1 and R2, nodal analysis can be performed at the V^+ node terminal to find the R1/R2 ratio and assign the appropriate resistance values to R1 and R2 with the following computation:

$$I1 = I2$$

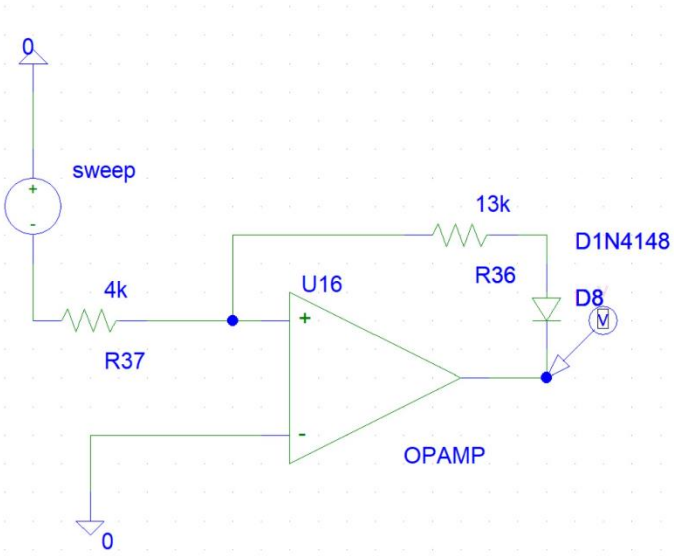
$$\frac{Vin - V+}{R1} = \frac{(V+) - Vout}{R2}$$

$$Vin = -Vout\left(\frac{R1}{R2}\right)$$

$$\frac{R1}{R2} = -\frac{Vin}{Vout}$$

$$\frac{R1}{R2} = -\frac{4}{(-13)} = \frac{4}{13}$$

With this R1/R2 ratio, we can assign the resistances to R1 = 4k Ohms and R2 = 13k Ohms, the issue is that if same design as Schematic 3 is applied then the switching points will be Vin1 = -4V when Vout = 13V and Vin2 = 4V when Vout = -13V and since we want to get rid of the -4V when our switching points are 4V and 0V then adding a diode pointing towards the output terminal right after R2 will help get rid of that -4V switching point ultimately giving us the other 0V switching point.



Schematic 4 - Circuits with Hysteresis Design Project A

As a result, when an input voltage sweep is applied, if the input voltage goes from +13V to -13V, as soon as the input voltage reaches 0V then the output voltage will go from +15V to -15V; on the other hand, if the input voltage goes from -13V to +13V, as soon as the input voltage reaches 4V then the output voltage will go from -15V to +15V. For step (14), the circuit had to be tested by sweeping the input voltage until the switching happened going from input voltage sweep of positive to negative and negative to positive. Tables 3 and 4 below display those input sweeps from positive to negative and negative to positive confirming our derived resistance values and added diode that give us those switching points.

Vin	**Vout**
3.89V	-14.89V

4.09V	+14.92V

Table 3 - Input Sweep from negative to positive noted switching points

Vin	**Vout**
0.12V	+14.91V
-0.23V	-14.90V

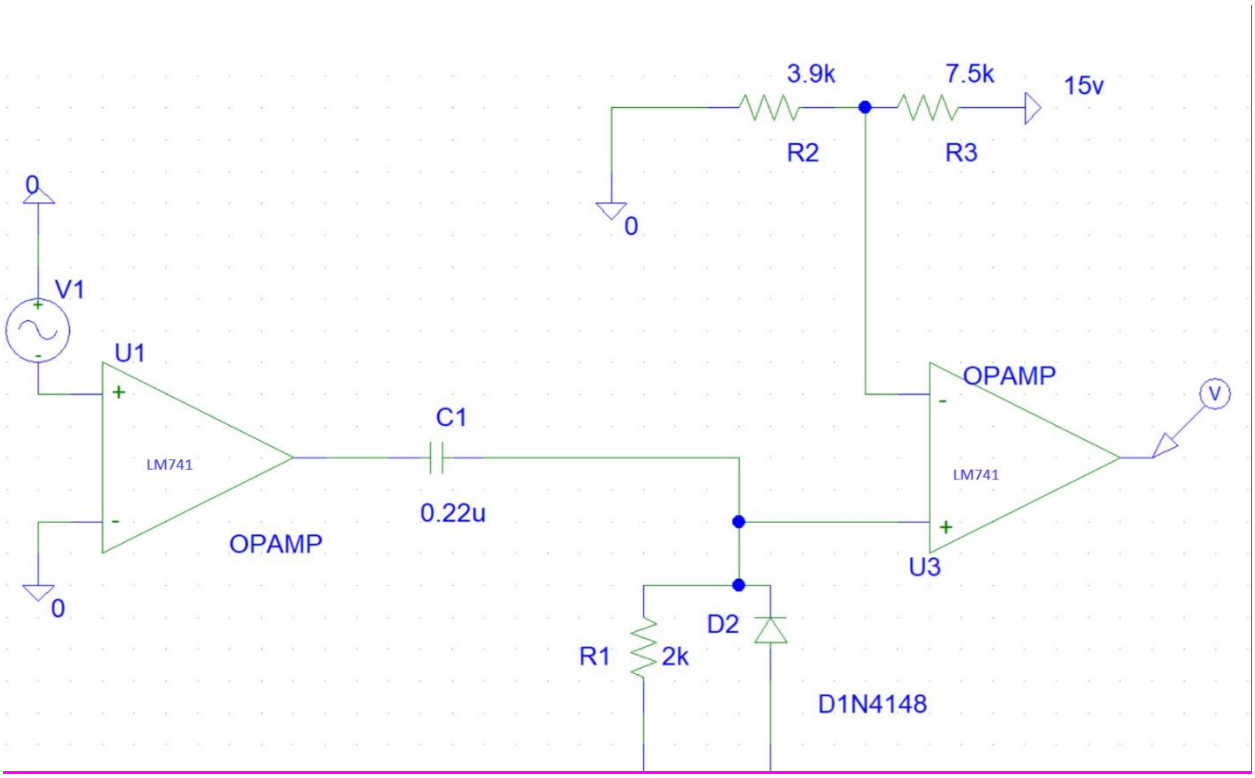
Table 4 - Input Sweep from positive to negative noted switching points

PULSE FORMING CIRCUITS

For this section of the lab, it was required to construct a pulse forming circuit with the given component specifications per project letter, since our group was assigned to project A then the following circuit parameters were given:

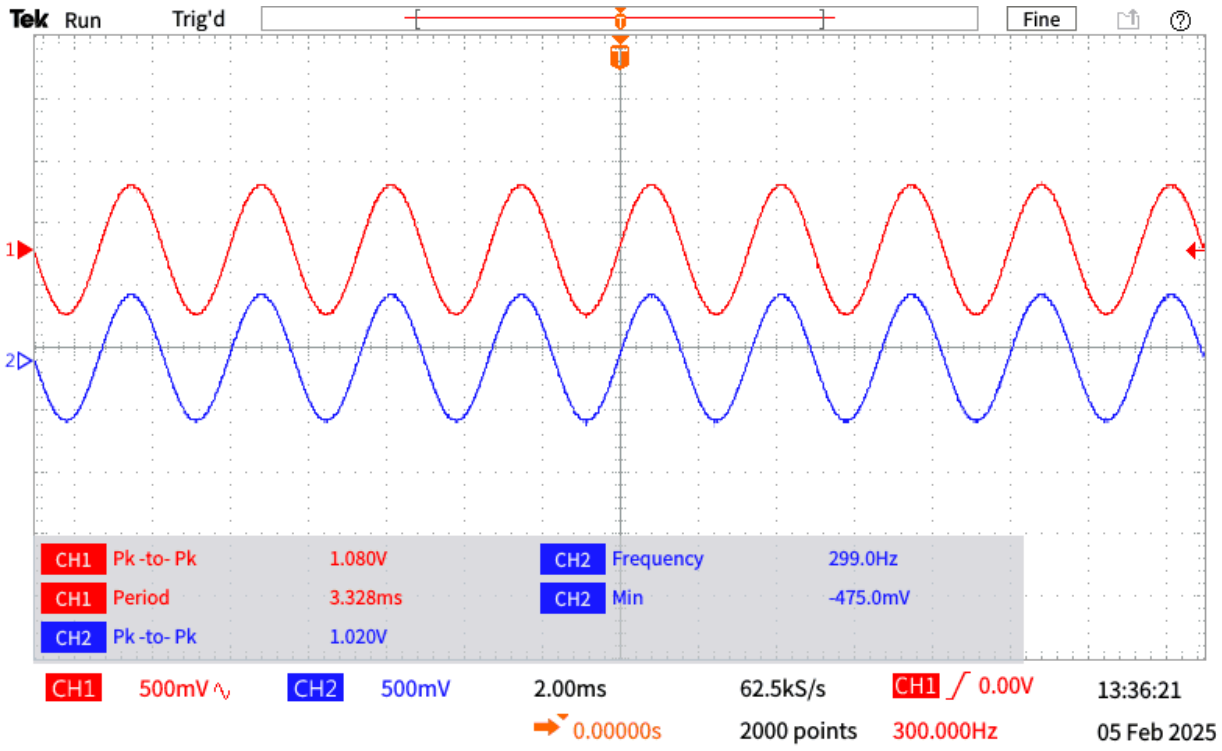
Project	**+VPS**	**-VPS**	**C1**	**R1**	**R2**	**R3**
A	+15	-15	0.22uF	2k	3.9k	7.5k

With the given parameters/component values, the circuit was constructed with two LM741 op amps and tested with a 300 Hz sine wave, 1V peak-to-peak, with no offset as the input voltage and take scope shots of points F, G, H, and J.



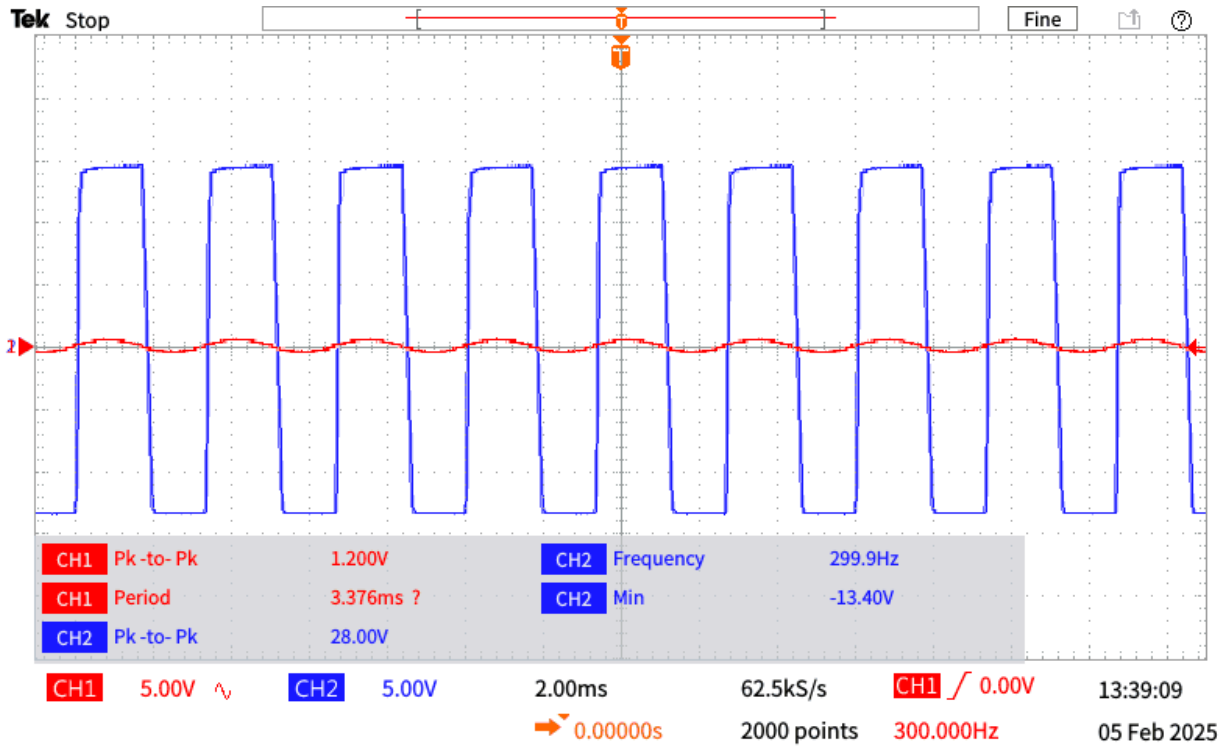
Schematic 5 – Pulse Forming Circuit Schematic

The reason for the output waveform at F input and output looking the same would be because both oscilloscope probes are measuring the same point at the function generator's circuit input so naturally, they will look the same.



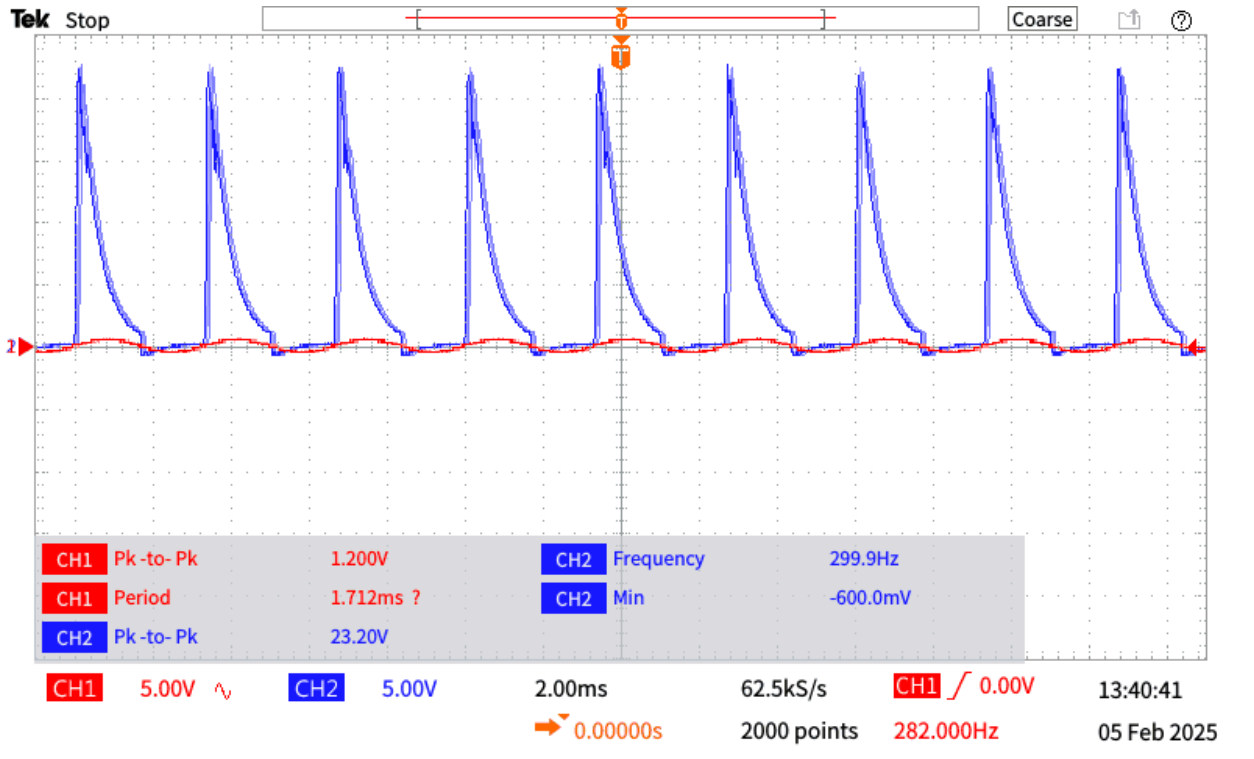
Scope Shot 7 - Pulse forming circuit Input (Red) and output waveform (Blue) at point F

The reason for the output waveform at G and why it looks like a square wave would be that, that is the output of the first op amp and it is switching at around the 0V input of the sine wave from +15V to -15V and -15V to +15V at the output shown in blue waveform below giving us a gain of around 14.6 V/V.



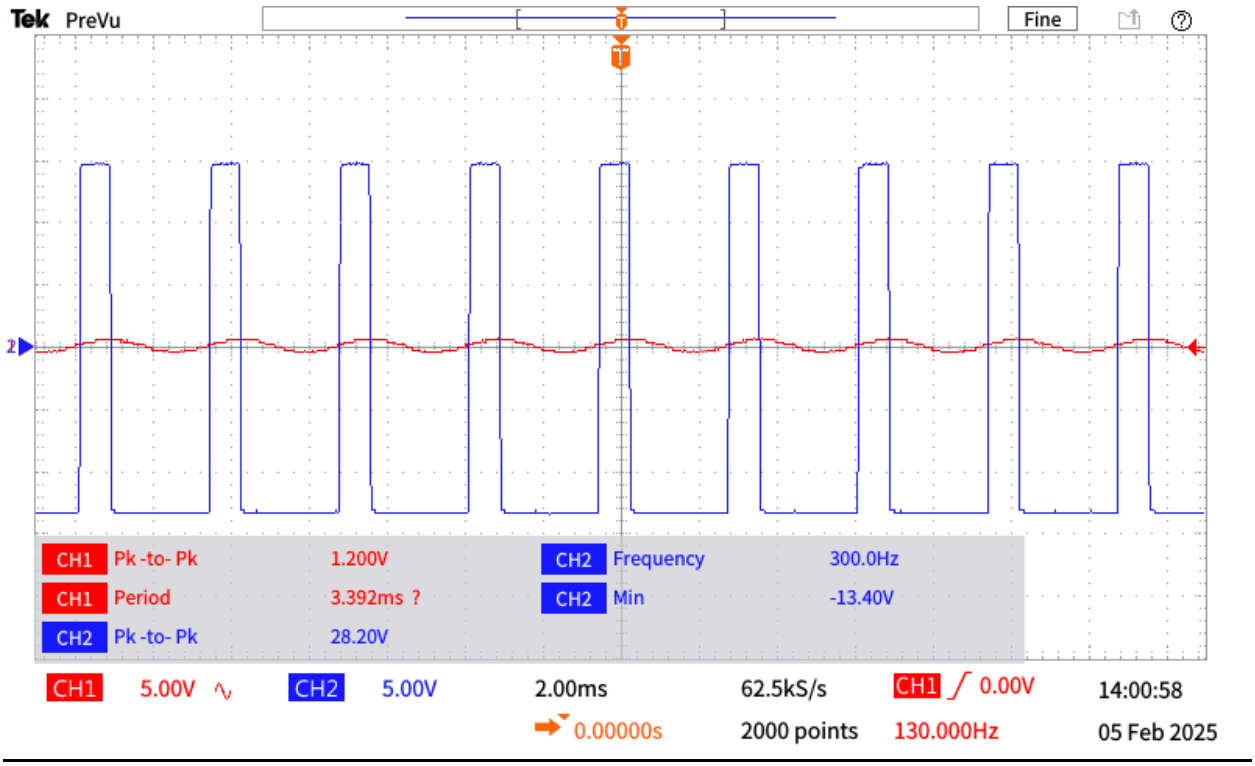
Scope Shot 8 - Pulse forming circuit Input (Red) and output waveform (Blue) at point G

The reason for the output waveform at H and why it peaks and slowly goes down would be due to the RC constant or more specifically the capacitor that is placed at the output along with the resistor that lets the capacitor discharge, since we have a 0.22 uF (0.2308 uF measured) capacitor and a 2k Ohm (1.97k measured) resistor then we can briefly calculate the RC time constant value to be ~ 0.4546 milliseconds.



Scope Shot 9 - Pulse forming circuit Input (Red) and output waveform (Blue) at point H

The reason for the output waveform at J would be that since the signal is being filtered by the last op amp, those peaks that we previously saw in scope shot 9 will be boosted by the second op amp giving us back a square waveform and a gain of 23.5 V/V.



Scope Shot 10 - Pulse forming circuit Input (Red) and output waveform (Blue) at point J

PULSE FORMING CIRCUITS – REDESIGN

For the redesign section of the pulse forming circuit part, it was required to redesign the previously given pulse forming circuit but with different parameters for project A:

Project	Pulse Width	Pulse Polarity	Low Value	High Value
A	220 us	Negative	-5V	0V

First off, to find out the values for R2 and R3 we know that we need to displace/offset the output wave -5V downwards meaning that we'll use the non-inverting terminal to move the waveform downwards by -5V. To do that, we'll swap the voltage divider at the R2 and R3 middle output to the non-inverting terminal of the second op amp and the first op amp's output to the inverting

terminal of the second op amp. With this information we can now calculate the values for R2 and R3 with the R2/R3 ratio from doing nodal analysis at the non-inverting terminal V^+ which we'll call V.

Nodal at $V^+ = V$

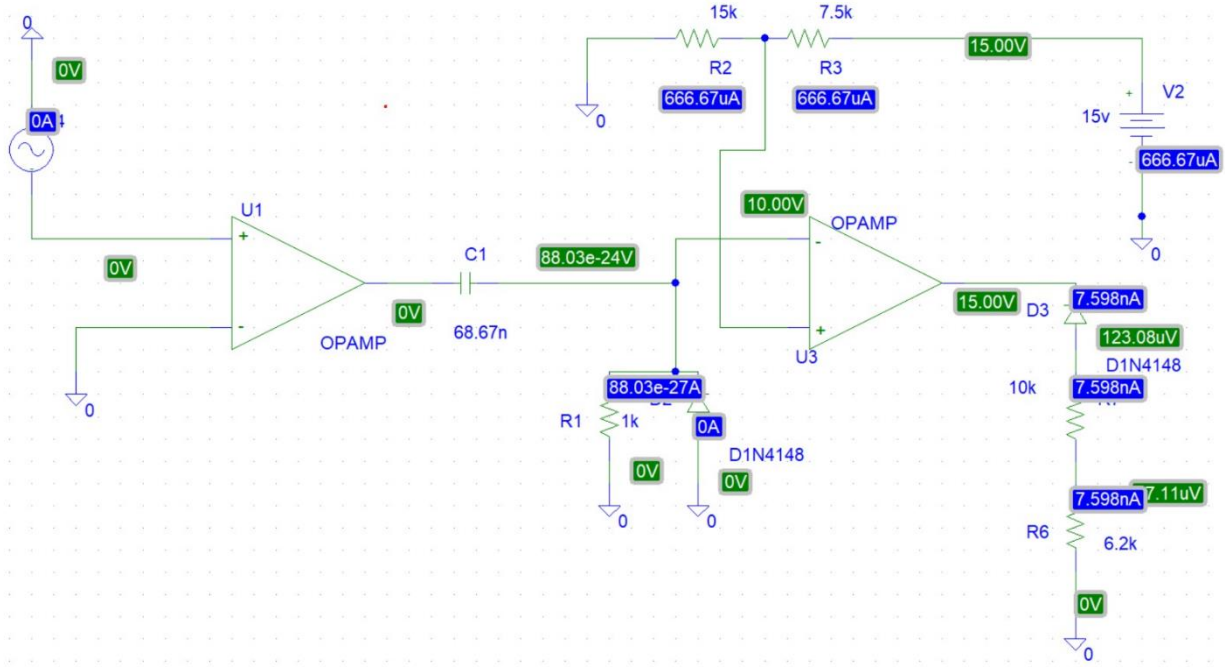
$$I3 = I2$$

$$\frac{15 - V}{R3} = \frac{V}{R2}$$

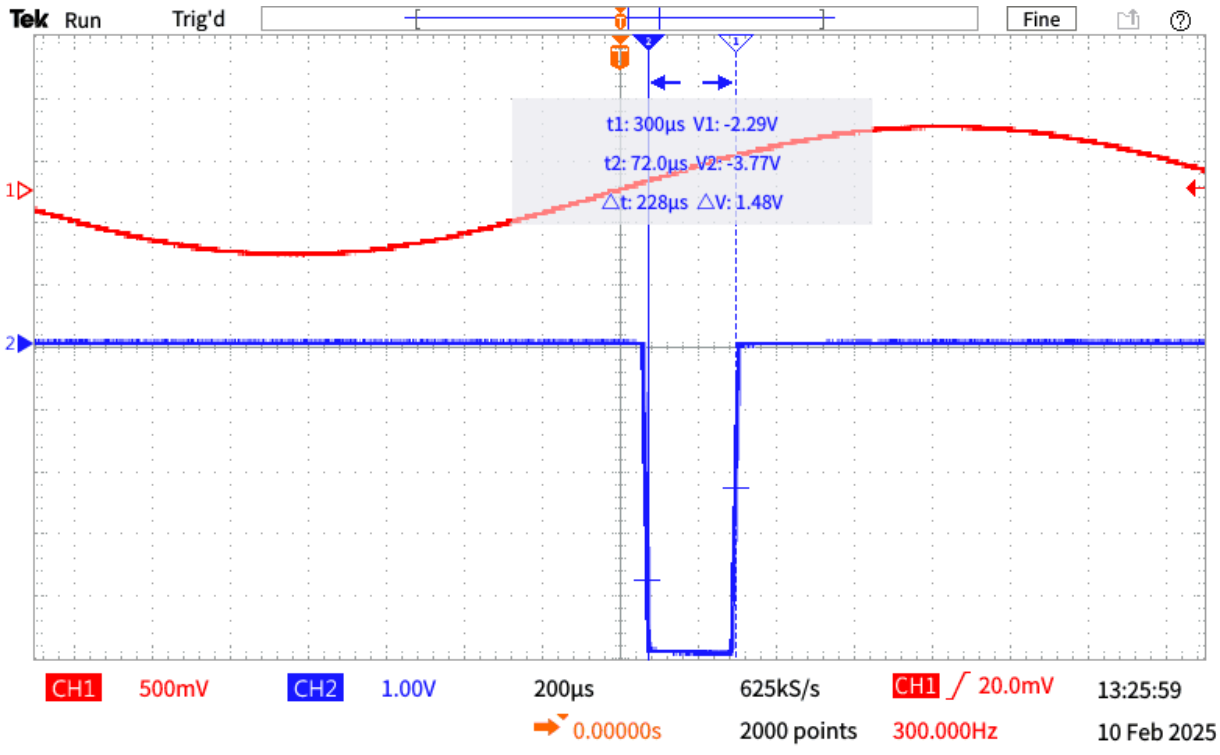
$$\frac{15 - 5}{R3} = \frac{5}{R2}$$

$$\frac{R2}{R3} = \frac{1}{2}$$

With this ratio, the appropriate resistances for R2 and R3 can be assigned as R2 = 15k (14.85k measured) ohms and R3 = 7.5k ohms (7.34k measured), for R1 and C1 we made it smaller until we got the right pulse width as we know that the smaller the RC value, the smaller pulse width at the output waveform which we chose R1 = 1k ohs and C1 = 68.67 nF. Since we wanted to control the output to be not +15V and -15V but 0V high and -5V low with the already mentioned displacement of 5V, it was decided to add a diode going into the second op amp to get rid of the positive output and splitting the voltage to get -5V at the output. To get 5V at the output between R7 and R6 was simple we picked R7 to be 10k ohms to drop 10 volts and 6.2k ohms for R6 to display 5V at the desired output between those two resistors, the reason why we picked 6.2k instead of 5k would be because we noticed that the output wasn't displaying -5V correctly so we increased the resistance to get better results which the scope shot and schematic will be displayed below.



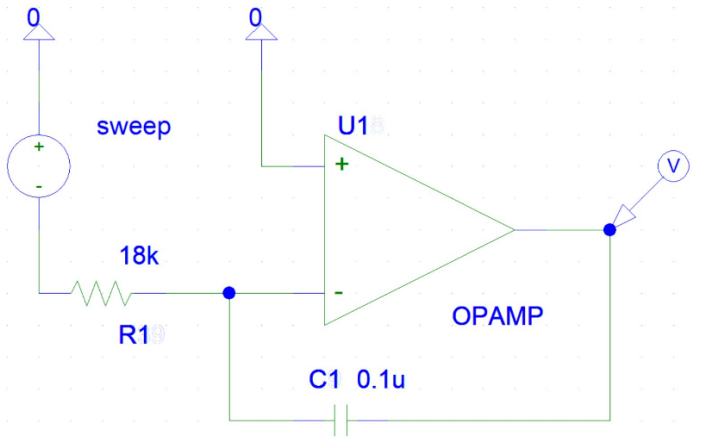
Schematic 6 - Pulse Forming Circuits Redesign



Scope Shot 11 - Pulse forming circuit redesign Project A with desired parameters of output (Blue)

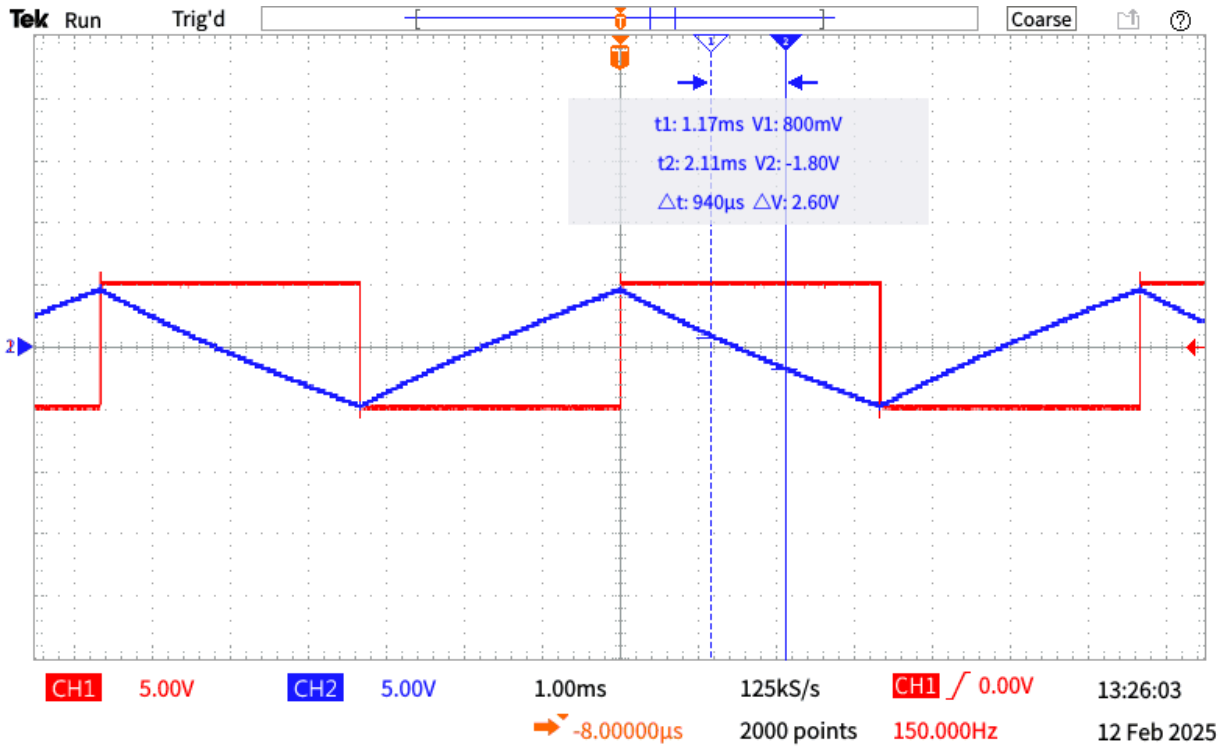
MILLER INTEGRATOR AND WAVEFORM GENERATOR

For the Miller integrator and waveform generator section of lab 1, it was required to build the given Miller integrator circuit with the specified component values for C1 = 0.1 uF and R1 = 18k ohms for project A.



Schematic 7 - Miller Integrator Circuit Schematic

For step (20), it was asked to test the built circuit with a 10 peak-to-peak square wave, 150 Hz, no offset and check the input and output on an oscilloscope. The following scope shot displays the input and output after the given parameters:



Scope Shot 12 - Miller Integrator and waveform generator input (Red) and output (Blue)

For step (21), it was asked to compute the theoretical slope for the output wave and compare to measurements. To calculate for the output voltage Vout, we can use nodal analysis at the inverting terminal of the op amp to find out the output voltage slope:

Nodal Analysis at V^- Terminal

$$I1 = I2$$

$$\frac{Vin - V-}{18000} = C\left(\frac{dv(t)}{dt}\right) \ (Replacing\ I2\ with\ capacitor\ Current\ eq.)$$

$$\frac{Vin - 0}{18000} = C * \frac{d}{dt} * (V - Vout)\ (Replacing\ V- = 0V\ since\ there's\ Negative\ Feedback)$$

$$\frac{Vin}{18000} = C * \frac{d}{dt} * (-Vout)$$

$$Vout = \int -\frac{Vin}{C} * 18000\,dt\ (Isolate\ Vout\ using\ Algebra\ and\ Calc\ 2)$$

$$Vout = -\frac{Vin}{C * 18000}\int 1\,dt$$

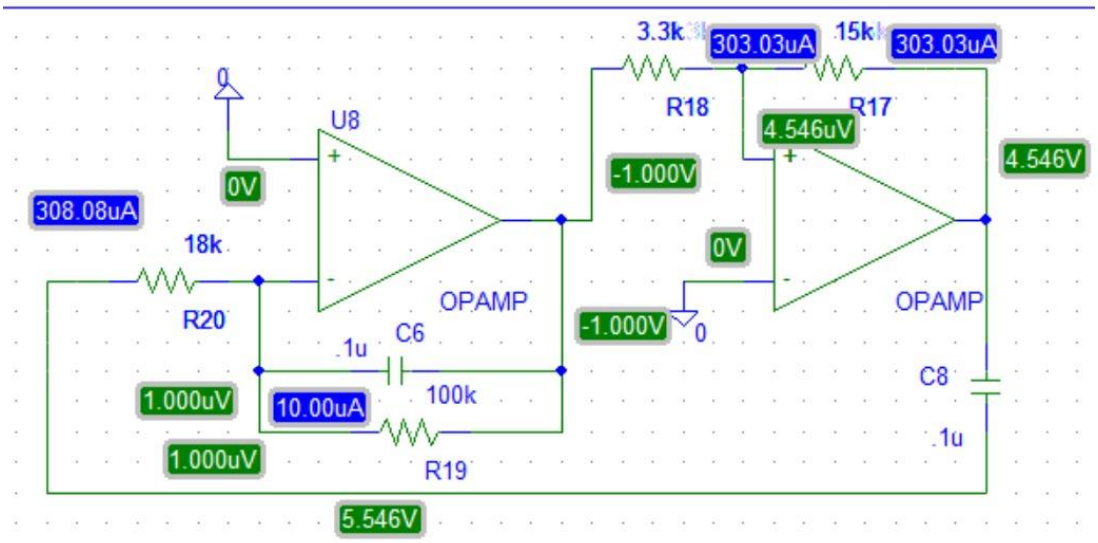
$$Vout = -\frac{Vin}{(0.1 * 10^{-6})(18000)} * t\ \ (Replace\ C = 0.1 * 10^{-6})$$

$$Vout = -\frac{Vin}{1.8 * 10^{-3}} * t$$

$$Vout = -\frac{5}{1.8 * 10^{-3}} * t = -2880t\ \ \ (Replace\ Vin = 5V\ to\ get\ negative\ slope)$$

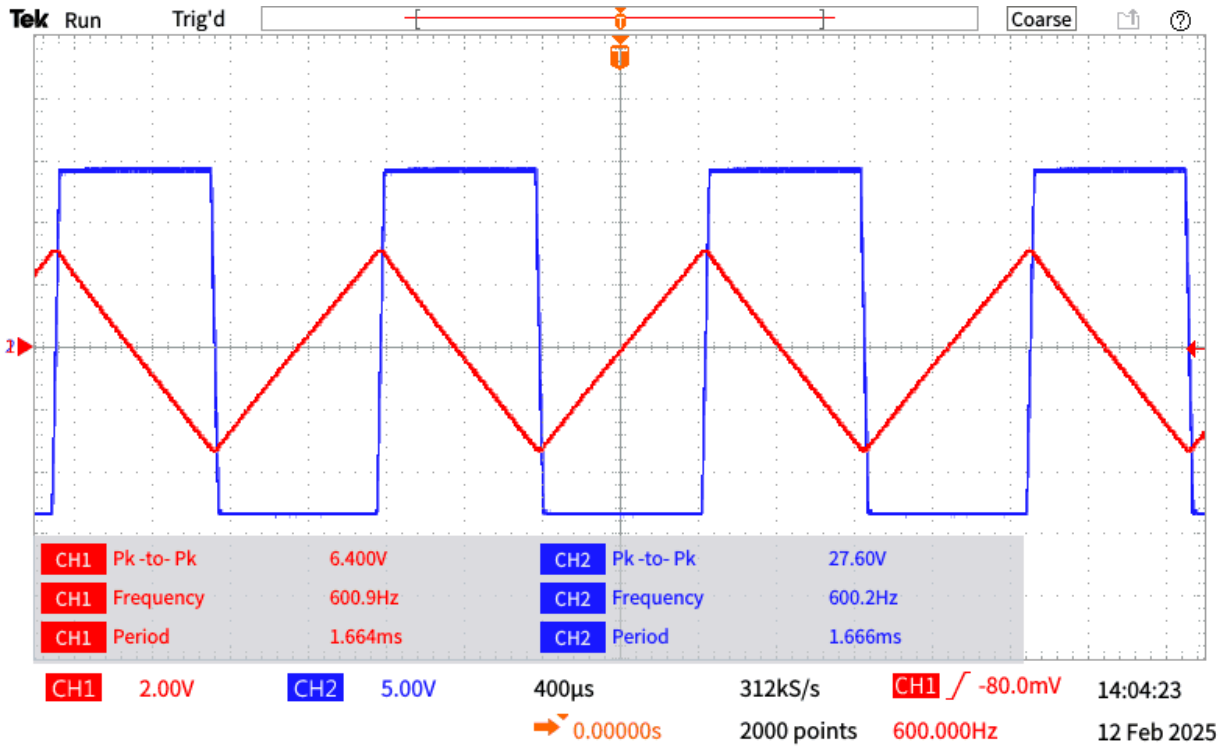
$$Vout = -\frac{(-5)}{1.8 * 10^{-3}} * t = 2880t\ \ (Replace\ Vin = 5V\ to\ get\ positive\ slope)$$

With the recently derived slope values we can compare to the measured ones by simply getting the rise/run of the voltage/seconds shown on the oscilloscope displayed on “Scope Shot 12”, and by simply computing the slope = voltage/seconds = 2.60V/940 us = 2765 which is close to or calculated value. This measured slope of 2765 is true for the negative and positive meaning that the negative slope would be around -2765. To compute the frequency for the Miller Integrator would be by using the following formula f = 1/4RC = 1/(4)(1.73558*10^-3) = 144 Hz which is 6 Hz off the measured frequency displayed on “Scope Shot 12”. For step (22), it is instructed to add a hysteresis circuit to the Miller integrator that was just built with the also given component values which the resulting circuit schematic for the Miller Integrator + Hysteresis Circuit will be displayed below:



Schematic 8 - Miller Integrator + Hysteresis Circuit

The recorded waveform for the output 1 which would be on the right side of capacitor C6 and output 2 which would be at the output of the second op amp will be displayed below:



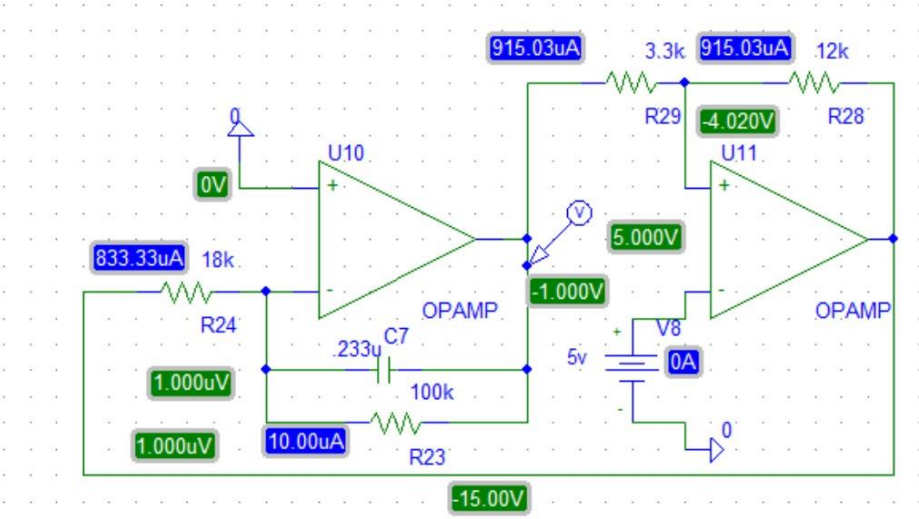
Scope Shot 13 - Miller Integrator + Hysteresis Circuit Output 1 (Red) and output 2 (Blue)

The calculated Miller Integrator + Hysteresis frequency would be by using the following formula which gives us a frequency extremely close to the measured 600 Hz displayed on “Scope Shot 13” also the computed amplitudes match as the displayed amplitude on oscilloscope is of 3.2V for output 1 and 13.8V for output 2:

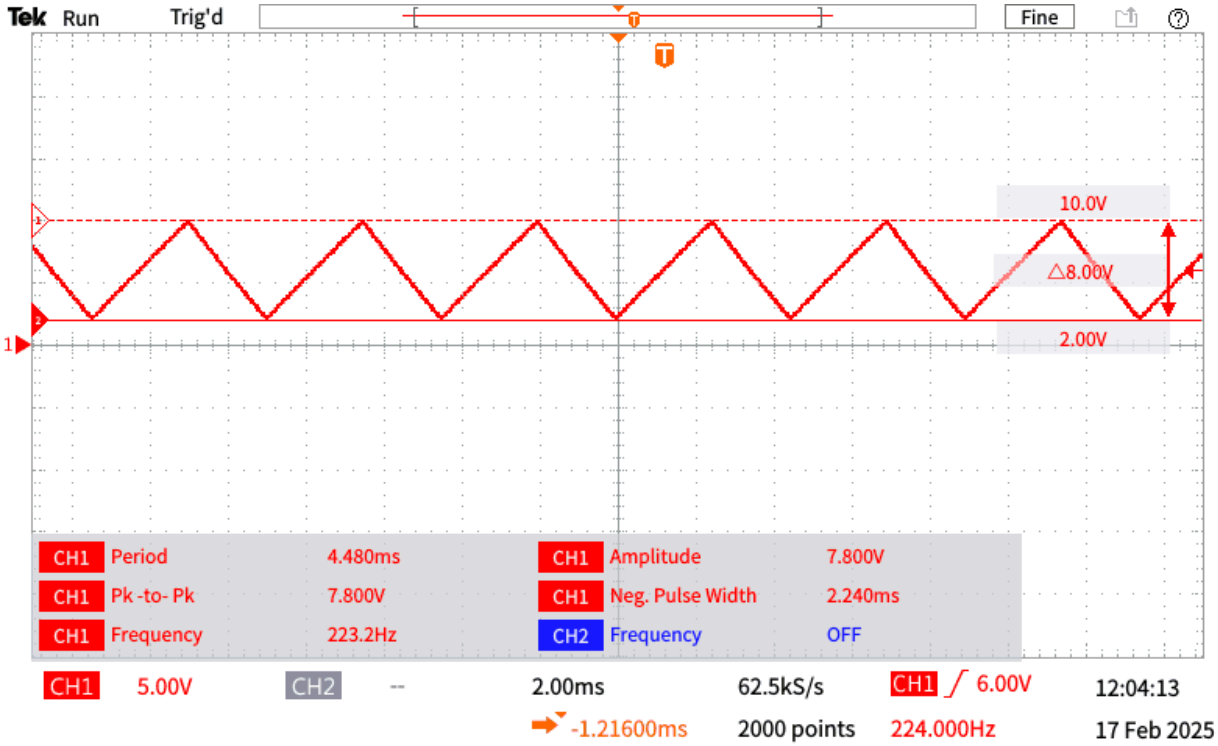
$$f = \frac{1}{4.3 * R * C\left(\frac{R2}{R3}\right)} = \frac{1}{4.3(1.73558 * 10^{-3})(\frac{3300}{15000})} = 609\ Hz$$

DESIGN PROBLEM – WAVEFORM GENERATOR

For the last section of lab 1, it was instructed to design a waveform generator depending on the project letter given, since our group got assigned project A, the requirements were to have a ramp waveform with a frequency of 220 Hz and 8V peak-to-peak with an offset starting at 2V which will get the waveform amplitude to be from 2V to 10V. To achieve this waveform, the same Miller Integrator + Hysteresis Circuit was used from the previous section “Schematic 6” and only focused on output 1 which will give us the ramp waveform displayed on “Scope Shot 13” as the red waveform. The original waveform had a peak-to-peak waveform of 6.4V but we need 8V, therefore we changed R28 to be 12k ohms instead of the previous 15k ohms to increase amplitude to 8V giving us +4V and -4V at the origin. To change the frequency, more capacitance was added in parallel to the only capacitor in the circuit to slow down the overall frequency which we ended up getting a capacitance of 0.233uF giving us a frequency of 224 Hz. To finally offset the voltage to not be at the origin but to start at 2V – 10V we added 5V to the inverting terminal of the second op amp as a reference voltage which will displace the output voltage upwards to our desired 2V start to 10V. Everything else in the circuit remained the same from the previous “Schematic 6”. Scope shot and circuit schematic will be shown below:



Schematic 9 – Design Problem Waveform Generator Project A



Scope Shot 14 - Design Problem Ramp Waveform Generator Project A

III. SUMMARY OF RESULTS

Section	Specification	Measured/Observed
Input Voltage Source	−13 V to +13 V range	−13.2 V to +13.4 V
Comparators Using Standard Op-Amps	Threshold = −5 V ± 0.5 V	Threshold = -4.95 V = -5.07 V
	Output levels = 0 V, +9 V ± 0.5 V	Output = 0.05 mV = 9.234 V
	Upper-frequency limit	Frequency = 170k Hz
Comparator Using Comparator Integrated Circuit (LM311)	Threshold = −6 V ± 0.5 V	Threshold = -5.913 V = -6.093V
	Output levels = 0 V, +4 V ± 0.5 V	Threshold = 114.42 mV = 4.99 V
	Upper-frequency limit	Frequency = 150k Hz
Circuits with Hysteresis (Pre-Design)	Two switching thresholds	Vin1 = -7.66V (When Vout = +13V) Vin2 = 7.66V (When Vout = -13V)
Circuits with Hysteresis – Design	Thresholds at 0 V, +4 V ± 0.5 V	Vin1 = 0V Vin2 = 4V
Pulse Forming Circuits	Output shape at nodes F, G, H, J	As per figures/oscilloscope shots
Pulse Forming Circuits – Redesign	Pulse width = 220 µs ± 25 µs	Pulse Width = 228 uF
	Pulse high/low value= −5 V, 0 V ± 0.5 V	Pulse high/low value = ~ -5V, 0V
Miller Integrator and Miller Integrator + Hysteresis Circuit	Integrator slopes vs. theory	Measured Slope = ±2765t Theoretical Slope = ±2880t
	Hysteresis oscillation frequency, amplitude	Frequency = 150 Hz Frequency Calculated = 144 Hz Amplitude = 5 V
	Hysteresis + Miller Frequency, amplitude	Frequency = 600 Hz Frequency Calculated = 609 Hz Amplitude1 = 6.4 Amplitude2 = 27.6
Design Problem – Waveform Generator	220 Hz ± 20 Hz output (10 V to 2 V range)	224 Hz (10V to 2V range)

IV. CONCLUSION

In conclusion, this laboratory investigated several key nonlinear analog circuits, systematically verifying each design requirement. Starting with the Input Voltage Source, the potentiometer and buffer ensured a stable, wide-range voltage supply (approximately −13 V to +13 V) to drive subsequent comparator and trigger circuits.

For the Comparators Using Standard Op-Amps, results demonstrated that a conventional operational amplifier could detect thresholds (e.g., −5 V) and provide outputs at the required levels (0 V and +9 V), though it exhibited limited performance at higher input frequencies. In contrast, the Comparator Using a Comparator Integrated Circuit (LM311) achieved faster switching and cleaner transitions across a broader frequency range, confirming its suitability for dedicated threshold applications.

Experiments with the Circuits with Hysteresis (Schmitt Trigger) highlighted the principle of hysteresis, where two distinct switching thresholds eliminated output chatter in noisy environments. The Hysteresis Design portion demonstrated how feedback network modifications (including diodes, offset references, and specific resistor ratios) could set asymmetrical trigger points of 0 V and +4 V accurately.

In the Pulse Forming Circuits, standard op-amp configurations with RC networks generated sharp pulses from a low-level sine wave input, while the Pulse Forming Circuits – Redesign revealed the precision needed in selecting capacitor and resistor values (and potential biasing) to ensure the specified −5 V to 0 V pulse amplitude and the 220 µs timing requirement.

Finally, with the Miller Integrator and Waveform Generator, the integrator's output slope was validated against theoretical predictions, demonstrating how capacitor and resistor selections control the integration rate. The addition of a hysteresis loop produced a free-running relaxation oscillator. Extending this approach into the Design Problem – Waveform Generator, a standalone circuit was realized that generated a 220 Hz output waveform with a specified amplitude range (10 V peak to 2 V trough), further illustrating how feedback and offset adjustments can achieve target frequencies and voltages within tight tolerances.

Overall, these experiments underscored several fundamental lessons:

Threshold Detection – Standard op-amps can act as comparators but are limited in speed, whereas dedicated comparators (LM311) excel in high-frequency or more demanding applications.

Hysteresis and Schmitt Triggers – Intentional positive feedback creates stable multi-threshold behavior critical to noise rejection.

Pulse Shaping – Selecting RC values precisely is crucial for generating pulses of desired amplitude and width.

Waveform Generation – Combining integration with hysteresis can form a self-sustaining oscillator whose frequency and amplitude are set by component values.

From the initial input source to the final waveform generator design, each step illustrated the power and flexibility of analog circuitry in creating signals and controlling switching behavior within well-defined specifications.